Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A process for estimating power consumption, over a given time interval, of a digital circuits described at ~~the~~ a level of a simulated functional elements provided with input/output terminals, ~~characterized in that it comprises the operations of~~the process comprising:

estimating the power consumption based on a number of transitions performed by the simulated functional element during said time interval, including:

emulating, at ~~the~~ a hardware level corresponding to an abstraction level of the digital circuit, additional elements associated to said functional ~~elements;~~ element, said additional emulated elements being able to detect, during emulation of the digital circuit, at least one signal indicative of ~~the~~ a behavior, and hence of power consumption, of the ~~corresponding~~ functional element associated during said time interval; and

acquiring ~~the~~ a value of said at least one signal, said value being indicative of the number of transitions and usable to determine ~~of~~ the power consumption of said associated functional element in said given time interval.

2. (Currently Amended) The process according to claim 1~~,~~ wherein said additional elements are emulated by associating them to an output of the ~~respective~~ functional element.

3. (Currently Amended) The process according to claim 1~~,~~ wherein said additional emulated elements are able to detect, during said given time interval:

~~the number of transitions performed by the corresponding associated functional element; and~~

~~the~~ a fraction of time in which ~~the~~ a state of the ~~corresponding~~ associated functional element is stable,

the value of said number of transitions and said fraction of time being indicative of the power consumption of said functional element during said time interval.

4. (Currently Amended) The process according to claim 1, ~~wherein it comprises the operation of~~further comprising controlling ~~the~~ acquisition of the value of said at least one signal ~~by means of~~ using hardware events monitored by logic analyzers active on the ~~emulator~~additional elements.

5. (Currently Amended) The process according to claim 1, ~~wherein it comprises~~further comprising ~~the operation of~~ accessing ~~the~~ information stored in said additional emulated elements and ~~the operation of~~ storing said information in view of a subsequent processing.

6. (Currently Amended) A processing system configured ~~for the implementation of~~to implement the process according to claim 1.

7. (Currently Amended) A computer program product directly loadable into ~~the~~ an internal memory of a digital computer, comprising software code portions ~~for performing the~~to perform the process ~~steps~~ of claim 1 when said product is run on ~~a~~ the computer.

8. (New) The process of claim 1 wherein emulating at the hardware level includes emulating at a register transfer level (RTL).

9. (New) The process of claim 1 wherein emulating at the hardware level includes emulating at a gate level.

10. (New) A system for estimating power consumption, over a given time interval, of a digital circuit described at a level of a simulated functional element provided with input/output terminals, the process comprising:

means for emulating, at a hardware abstraction level corresponding to an abstraction level of the digital circuit, an additional element associated to the functional element, the additional emulated element being able to detect, during emulation of the digital circuit, at least one signal indicative of a behavior of the functional element associated during the time interval; and

means for acquiring a value of the at least one signal, the value being indicative of the number of transitions performed by the simulated functional element during the time interval; and

means for estimating the power consumption based on the acquired number of transitions performed by the simulated functional element during the time interval.

11. (New) The system of claim 10 wherein the additional element is able to detect, during the given time interval, a fraction of time in which a state of the associated functional element is stable, the means for estimating using the value of the number of transitions and the fraction of time to determine the power consumption of the functional element during the time interval.

12. (New) The system of claim 10 wherein the hardware abstraction level is an RTL level or a gate level.

13. (New) An apparatus to estimate power consumption, over a given time interval, of a digital circuit described at a level of a simulated functional element provided with input/output terminals, the apparatus including comprising:

a first module to emulate, at a hardware abstraction level corresponding to an abstraction level of the digital circuit, an additional element associated to the functional element, the additional emulated element being able to detect, during emulation of the digital circuit, at

least one signal indicative of a behavior of the functional element associated during the time interval;

a second module operatively coupled to the first module to acquire a value of the at least one signal, the value being indicative of the number of transitions performed by the simulated functional element during the time interval;

a third module operatively coupled to the second module to estimate the power consumption based on the acquired number of transitions performed by the simulated functional element during the time interval.

14. (New) The apparatus of claim 13 wherein the additional element is able to detect, during the given time interval, a fraction of time in which a state of the associated functional element is stable, the third module being operative to use the value of the number of transitions and the fraction of time to determine the power consumption of the functional element during the time interval.

15. (New) The apparatus of claim 13 wherein the third module includes machine-readable instructions stored on a machine-readable medium and executable by a processor.

16. (New) The apparatus of claim 13 wherein the wherein the hardware abstraction level is an RTL level or a gate level.